REMARKS

Claims 1 - 7 remain active in this application. The specification has been reviewed and editorial revisions made where seen to be appropriate. Claims 1, 2 and 4 - 7 have been amended to improve form and/or for emphasis. New claim 8 has been added. Support for the amendments of the claims is found throughout the application, particularly in Figures 2, 4 - 7 and 10 and the description thereof in the specification, particularly on pages 12 - 16. No new matter has been introduced into the application.

The Examiner has objected to the drawings under 37 C.F.R. §1.84 as containing reference numerals 41, 49 and 50, not found in the specification. This objection is respectfully traversed as moot in view of the amendments to the specification made above in which reference numerals 41, 49 and 50 have been added at appropriate locations.

The Examiner has further objected to the drawings under 37 C.F.R. §1.83 as failing to illustrate claim 4 and rejected claim 4 under 35 U.S.C. §112, first paragraph, as being unsupported by enabling disclosure. This objection and rejection are respectfully traversed.

It is respectfully submitted to be well-accepted nomenclature and terminology in the art to refer to a single structure connecting respective regions or structures of different transistors (which are particularly common in matrix arrays such as memories where the common gate connections and common source drain connections form respective word and bit lines) as "common" or "shared" such as "shared gate" or "shared drain". In the case of the embodiment of the present invention shown in Figure 6 and 7, a plurality of transistors are connected in parallel for increased current carrying capability as schematically shown in

Figure 8 or in plan view in Figure 6 and thus have electrically common or shared sources, gates and drains. Specifically, as discussed on pages 14 and 15 of the specification in regard to Figure 6, particularly at page 15, lines 9 - 27, where it is explicitly disclosed that Q11 and Q12 share a common drain diffused region 125 and drain wiring 126, Q12 and Q13 share a common source diffused region 128 and common source/gate wiring 129, and so on through Q14. The drain wiring and source/gate wiring for each pair of transistors is also commonly connected in respective integral structures and are thus also "common" or "shared". Therefore, it is clear that the Examiner is incorrect in regard to both the objection and rejection since an enabling disclosure and clear illustration are clearly provided for a plurality of transistors having shared gates and drains. However, to even more clearly resolve these issues and in response to the appearance that the Examiner may be asserting that the *effective region* of the gates of different transistors cannot be in the same place but must be located in accordance with channel regions which are necessarily spaced from each other, claim 4 has been amended to refer to shared gate and drain *structures*. Accordingly, reconsideration of this objection and this rejection are respectfully requested.

The Examiner has objected to the Title of the application as being insufficiently descriptive. This objection is respectfully traversed as being moot in view of the above amendments which include substitution of a new and highly descriptive Title at all occurrences in the application. Accordingly, reconsideration and withdrawal of this objection is respectfully requested.

The Examiner has also objected to claim 6 as containing a misspelling. This objection is also respectfully traversed as being moot in view of the

above amendments which contain a correction of the spelling of "diffused". Therefore reconsideration and withdrawal of the objection are respectfully requested.

Claims 1 - 6 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite due to ambiguous antecedent reference using the pronoun "its". This rejection is respectfully traversed as being moot in view of the above amendments to claim 1 which clarify the reference in accordance with the Examiner's stated assumption. The Examiner's diligence in making that assumption is appreciated. Accordingly, reconsideration and withdrawal of this ground of rejection are respectfully requested.

Before proceeding to a discussion of the numerous asserted grounds of rejection based on prior art, the invention will now be summarized. The invention is directed to providing protection from electrostatic discharge (ESD) damage to a semiconductor device such as an integrated circuit. Such a circuit must provide for rapid response time, high current carrying capability and relatively low impedance when conductive. The protective circuit must also, as a practical matter, have a very small footprint since it is often preferred, for best protection, to provide a substantial number of such protective circuits surrounding a protected circuit (referred to as an internal circuit, largely for that reason). Diodes and FETs are each known for use as protective circuits and each has respective advantages as compared with the other. For example, a diode responds quickly to a potential pulse with a sharp rise in current but has a relatively high impedance. An FET has a relatively slow response time but relatively lower conductive impedance. Therefore, either device alone provides less than optimal performance for all electrostatic discharge circumstances but either may be adequate for particular conditions of electrostatic discharge.

However, both FETs and diodes must have a relatively large conductive area in order to minimize internal impedance and maximize current carrying capability. Therefore, either presents a trade-off between quality of ESD protection and chip area required and generally requires a diode or an FET to be used to the exclusion of the other. Conversely, if a parallel combination of a diode and an FET were to be used together to provide both rapid response (through the diode) and low conduction impedance (through the FET) the area penalty would be multiplied for a given current carrying capability and conduction impedance. The invention provides a combination of a diode and an FET for ESD protection in which current carrying capability may be enhanced while the area required may be held to only a slightly greater area than that required for the FET alone while reducing conduction impedance and increasing current carrying capability as well as greatly increasing withstand voltage of the FET with no significant area penalty and providing the performance advantages of both diode and FET protection from ESD damage. In this latter regard, it must be borne in mind that even ESD protective circuits can potentially be destroyed by sufficiently high voltages and/or currents. With the above as background, the grounds of rejection asserted by the Examiner will now be answered in turn. It is Applicants' position than none of the prior art relied upon by the Examiner teaches or suggests the subject matter of the invention or provides evidence of a level of ordinary skill in the art which would support a conclusion of obviousness or, in any way, lead to an expectation of success in providing a high level of ESD protection in a circuit of reduced chip area.

Claims 1 and 6 have been rejected under 35 U.S.C. §102 as being anticipated by Ker et al. This ground of rejection, which appears to be the basis for all

asserted grounds of rejection under 35 U.S.C. §103 relying on Ker et al. in combination with other prior art, is respectfully traversed.

Based upon the diagram provided by the Examiner, the boundary between P+ region 124 and N+ region 126 is considered to answer the recitation of a PN junction, as it, in fact, appears to be. (A similar PN junction appears between regions 114 and 116 of Ker et al.) However, the structure illustrated in Ker et al. does not answer the explicit recitations in claim 1 of "a diffused region ... forming a PN junction together with its periphery" (now "a diffused region ... forming a PN diode junction together with a periphery of said diffused region", as amended above), particularly as the "diffused region" has been construed in the diagram provided by the Examiner, or, perhaps more importantly, "wherein the field effect transistor and the PN diode junction are connected *between terminals* for absorbing excess current ..." (emphasis added) since regions 124 and 126 (and 114 and 116 are connected *together* in Ker et al. to function *together* as a low resistance cathode (or anode) of the SCR device to connect to The P-well (or N-well) rather than as a *junction* device such as a diode. Similarly, since region 108 (or 106) is construed to answer the "diffused region" recitation, it is unclear what region is considered by the Examiner to answer the "well region" recitation of claim 1. Moreover, the "diffused region" of Ker et al., as construed by the Examiner, extends to STI structure 134 and the junction is not formed at the periphery of the diffused region, as the Examiner has expressly interpreted the original claim language (which was subject to an asserted rejection under 35 U.S.C. §112, answered above and in regard to which the claim was clarified in accordance with the Examiner's assumption in regard to the language "its periphery" as discussed above).

Therefore, it is clear that Ker et al. does not, in fact, answer all recitations of claim 1 or claim 6 and does not anticipate any claim in the application. By the same token, it is clear from the diagram provided in the official action that the Examiner has not made and cannot make a *prima facie* demonstration of anticipation of any claim in the application. Moreover, by the above amendment, claim 1 (and depending claims making reference to the PN junction) have been amended to indicate that the junction is a diode junction which Ker et al. clearly cannot answer since the regions identified by the Examiner as forming the junction are connected together by Ker et al. to function as a contact region. Further, no modification of Ker et al. to answer the claimed subject matter can properly be proposed since provision of a diode junction would preclude the intended function of that structure in Ker et al., as discussed above (See In re Gordon, 221 USPQ 1125 (Fed. Circ., 1984)). Therefore this ground of rejection is now even more untenable and, upon reconsideration, should be withdrawn.

Claim 2 has been rejected under 35 U.S.C. §103 as being unpatentable over Ker et al. as applied to claims 1 (and 6) in view of the further teachings of Takao; claim 3 has been rejected under 35 U.S.C. §103 as being unpatentable over Ker et al. in view of Takao and Harari; claim 4 has been rejected under 35 U.S.C. §103 as being unpatentable over Ker et al. in view of Takao and Hirata; claim 5 has been rejected under 35 U.S.C. §103 as being unpatentable over Ker et al. in view of Hayashida et al. in view of Yamada et al. All of these asserted grounds of rejection are respectfully traversed since the Examiner has not demonstrated how any of the secondary references mitigate the clear deficiencies of Ker et al. discussed above, and thus has not made a *prima facie* demonstration of obviousness in regard to any claim in the application.

For example, in regard to claim 2, the Examiner admits that Ker et al. does not disclose a protective film and a conductive material formed thereon and relies on Takao for such teaching, citing Figure 1B. However, the Examiner does not mention the claim recitations of claim 1 in connection with provision of a diffused region forming a diode junction in combination with an FET transistor for a protection device. In regard to claim 3, the Examiner admits that Ker et al. and Takao do not teach or suggest the gate of the field effect transistor being made of metal and relies upon Harari for such teaching but, again, makes no mention of any relevance of Harari to the deficiencies of Ker et al. in regard to the claimed diode junction in combination with an FET. Similarly, in regard to claim 4, the Examiner admits that Ker et al. does not teach a plurality of transistors in a well region and relies on Hirata '354 for such a teaching without mentioning any relevance of Hirata to the deficiencies of Ker et al. In regard to claim 5, the Examiner admits that Ker et al. does not teach or suggest an impedance element and relies on Hayashida et al. for such a teaching and further on Yamada et al. and Sakamoto et al. for teaching a resistance device having a resistance larger than the conduction resistance of the protective circuit. However, the Examiner again fails to address the above-discussed deficiencies of Ker et al. Therefore, it is clear that the Examiner has failed to make a *prima facie* demonstration of obviousness of any of dependent claims 2 - 5 and the rejection of these claims is clearly improper for at least that reason and, upon reconsideration, should be withdrawn.

Claim 7 has been rejected under 35 U.S.C. §103 as being unpatentable over Ker et al. in view of Matsumoto. This ground of rejection is also respectfully traversed.

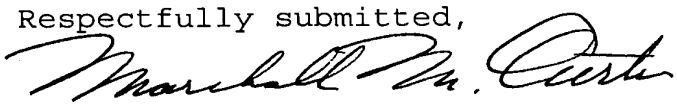
In regard to claim 7, the Examiner admits that Ker et al. does not teach an internal circuit connected to a plurality of terminals and relies on Matsumoto for teaching connections of an ESD protection device and an internal circuit to be protected. In regard to the recited constituent elements of the protection circuit, the Examiner asserts inherency in regard to the current response of the elements of Ker et al. However, it is respectfully submitted that an assertion of inherency is only proper when the functions asserted to be inherent necessarily result from the subject matter disclosed. As pointed out above in regard to claims 1 and 6, the regions forming the asserted PN junction of Ker et al. are connected together to function as a connection and thus not only do not produce the current response function of a diode but *cannot* function as a diode at all, much less inherently do so. Moreover, the device disclosed by Ker et al. is a silicon controlled rectifier, as noted by the Examiner, functioning as a single device and which must be controlled and thus is not and cannot function as a protective circuit at all much less a protective circuit comprising two elements and certainly not two elements having different current response characteristics. These deficiencies of Ker et al. to answer the recitations of claim 7 are not mitigated by Matsumoto which teaches little more than the connection of a protective circuit to an internal circuit as observed by the Examiner. Matsumoto is substantially silent in regard to the current response characteristics of the protective circuit. Therefore, it is clear that the combined teachings of Ker et al. and Matsumoto et al. do not answer the recitations of the claims and it is respectfully submitted that the Examiner's comments and observations clearly reflects impermissible hindsight and, in any event, do not answer the claim recitations, particularly as amended.

Therefore, in summary, it is seen that the Examiner has not made a *prima facie* demonstration of anticipation or obviousness in regard to any claim in the application regardless of the reference or combination of references applied and has clearly construed the reference through hindsight, improperly combined teachings including use of non-analogous art and suggestions erroneously determined and, moreover, appears to have ignored explicit recitations of the claims. Therefore, it is respectfully submitted that all of the various grounds of rejection asserted by the Examiner are clearly in error and untenable and reconsideration and withdrawal of the same are respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b). Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance.

A petition for a one-month extension of time has been made above. If any further extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,



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In the Drawings:

Please approve the proposed drawing revisions as shown in red in the attached sheets containing Figures 4, 5 and 8. Corresponding corrected formal drawing sheets are filed concurrently herewith.

FIG. 4

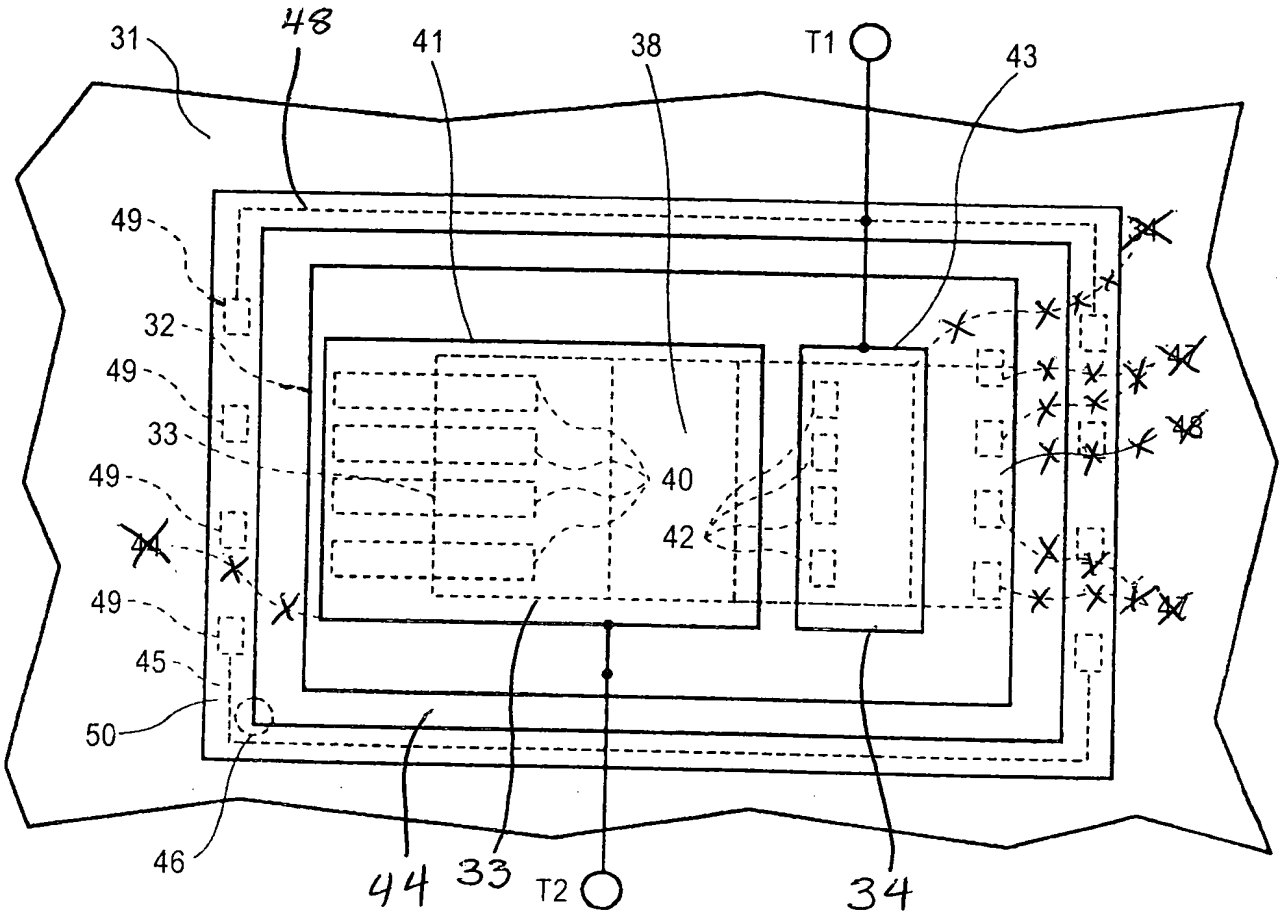

FIG. 5

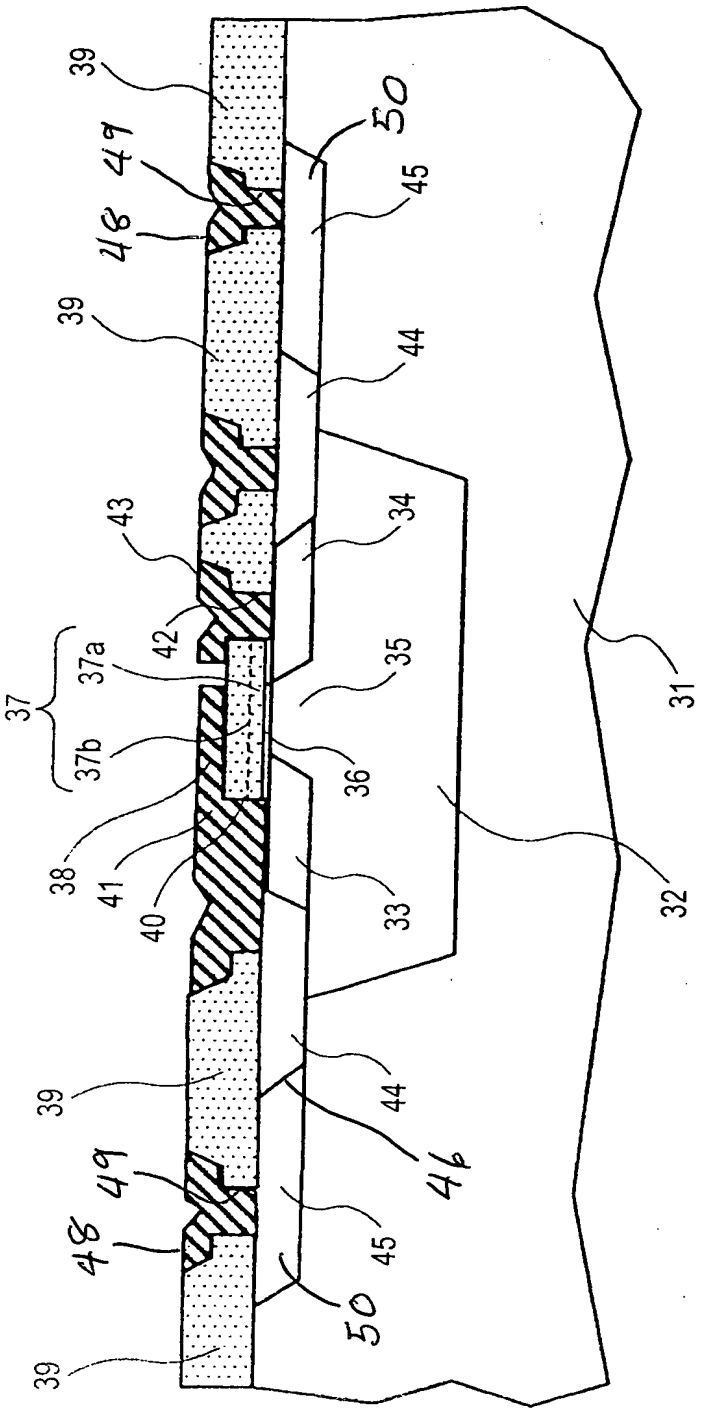

FIG. 7

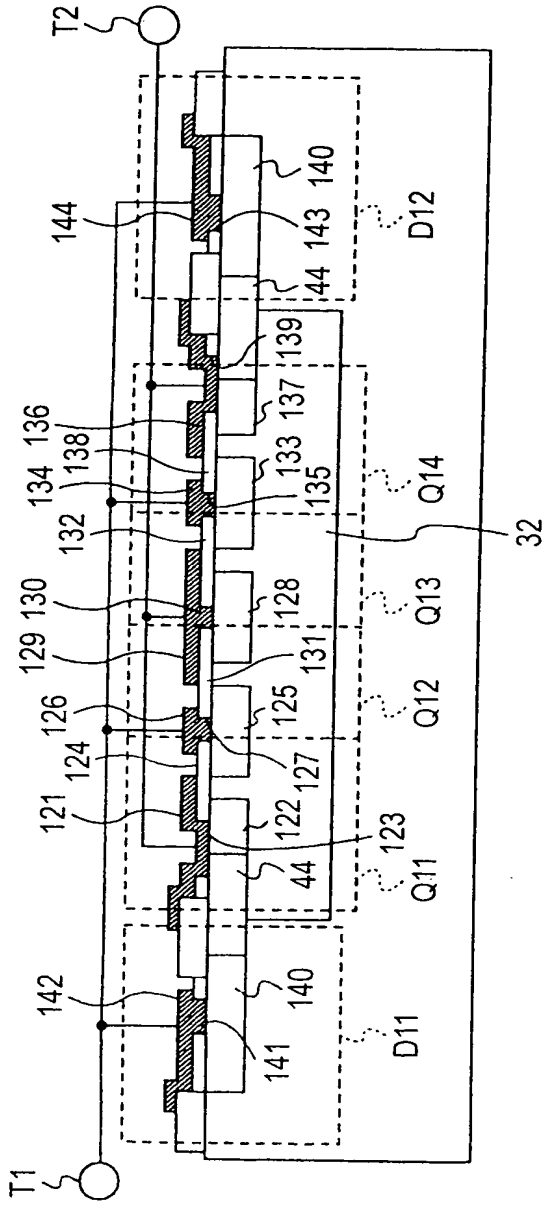

FIG. 8